PCB Layout and Design Guide for CH7525

4 Lane DispalyPort to HDMI 1.4 Converter

1.0 INTRODUCTION

Chrontel's CH7525 translates the DisplayPort signal to HDMI/DVI. This innovative DisplayPort receiver with an integrated HDMI Transmitter is specially designed to target the notebook/ultrabook, tablet device and PC market segments. Through the CH7525's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized multimedia data can be seamlessly converted to HDMI/DVI output.

The CH7525's DP/eDP receiver is compliant with the DisplayPort Specification 1.2a and the Embedded DisplayPort Specification version 1.3. With internal HDCP key Integrated, the device support HDCP 1.4 specifications. In the device's receiver block, which supports four DisplayPort Main Link Lanes input with data rate running at either 1.62Gb/s or 2.7Gb/s, can accept RGB digital formats in either 18 bit or 24-bit, and converted the input signal to HDMI output up to 1920x1080@120Hz or 3840x2160@30Hz. And the CH7525 support color depth 6/8/10/12bits. About audio the CH7525 can support up to 8-channel audio input from DP Rx and output from HDMI Tx with sample rate up to 192 KHz.

This application note focuses only on the basic PCB layout and design guidelines for CH7525. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 48-pin QFN (6x6 mm) package of the CH7525. Please refer to the CH7525 datasheet for the details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7525 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7525 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The CH7525 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7525 ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

Refer to **Table 1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7525 (QFN48)

Pin Assignment	# of Pins	Type	Symbol	Description
11,26	2	Power	DVDD	Digital Core/IO Power Supply (1.2V)
39,45	2	Power	AVDD	Analog Power Supply (1.2V)
1	1	Power	VDD_PLL	PLL Power Supply (1.2V)
10,27	2	Power	VDDS	Digital Serializer Power Supply (1.2V)
32	1	Power	AVCC	Analog Power Supply (3.3V)
13	1	Power	AVCC_PLL	PLL Power Supply (3.3V)
19	1	Power	VDDH	Analog HDMI Tx Power Supply(3.3V)
12,25	2	Ground	DGND	Digital supply ground
42	1	Ground	AGND	Analog supply ground
48	1	Ground	GNDPLL	PLL supply ground
16,22	2	Ground	VSSH	Analog supply ground
49	1	Ground	Thermal Pad	Power supply ground

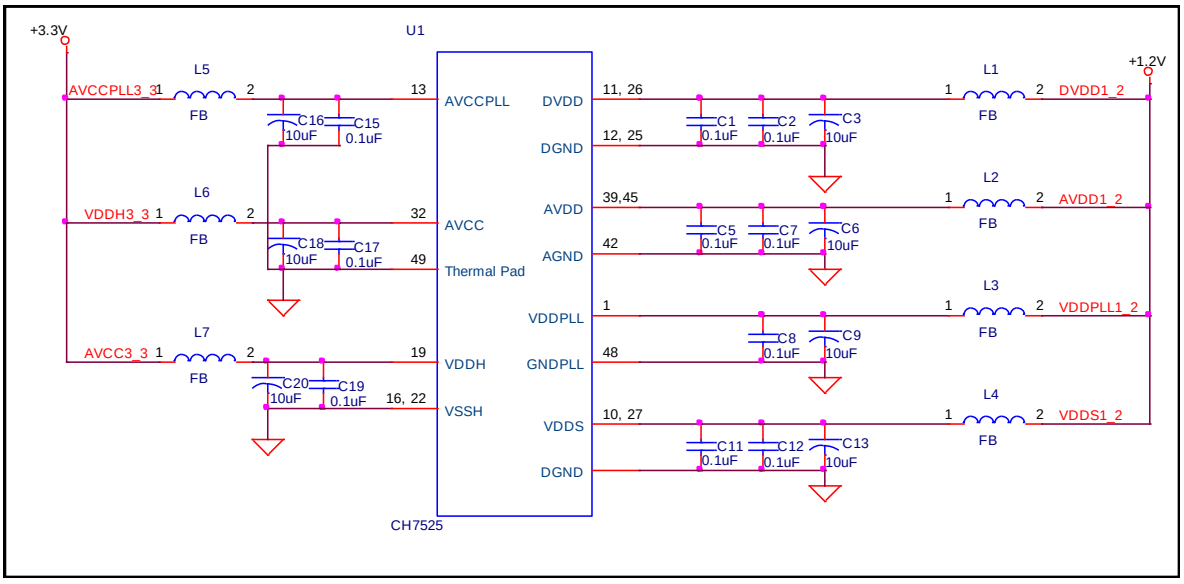

Figure 1: Power Supply Decoupling and Distribution

2.2 Internal Reference Pins

• RBIAS pin

This pin sets the Band-gap Bias Voltage. A 10 K-Ohm, 1% tolerance resistor should be connected between RBIAS and GND as shown in **Figure 2**. A smaller resistance will create less Band-gap Bias voltage. This resistor should be placed with short and wide traces as near as possible to CH7525. For optimum performance, this signal should not overlay the analog power or analog output signals.

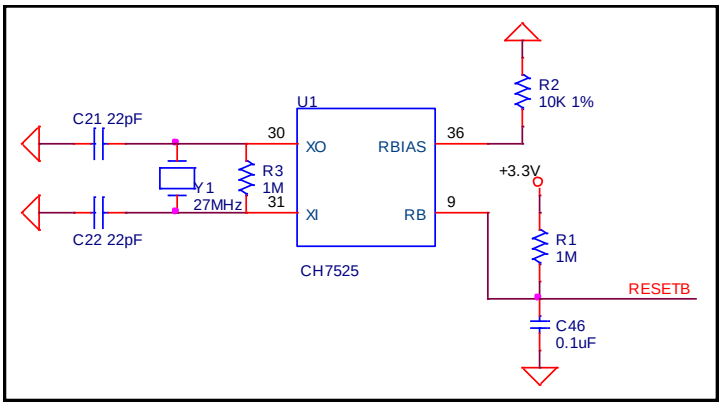

Figure 2: RBIAS Pin Connection and General Control

2.3 General Control Pins

• RSTB

This pin is the chip reset pin for CH7525. RSTB pin, which is internally pulled-up, places the device in the power on reset condition when this pin is low.
There are two methods for chip power-on reset.
1. The RB signal can be generated by on board Resistor and Capacitor delay, which can be refer to **Figure 2**.

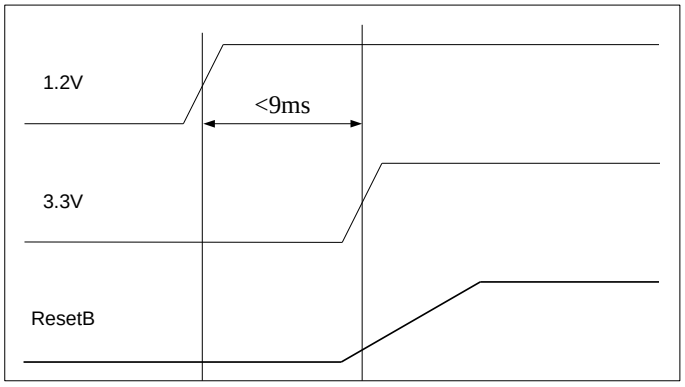

Figure 3: Power-on Reset Function's Sequence on board

Please note that the 1.2V power should be rise-up no later than the 3.3V power. Refer to **Figure 3.**

2. RB signal is generate by system global reset. In this case, the power supply should be valid and stable for at least 20ms before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. Otherwise, the chip can't work well. The timing is shown in **Figure 4.**

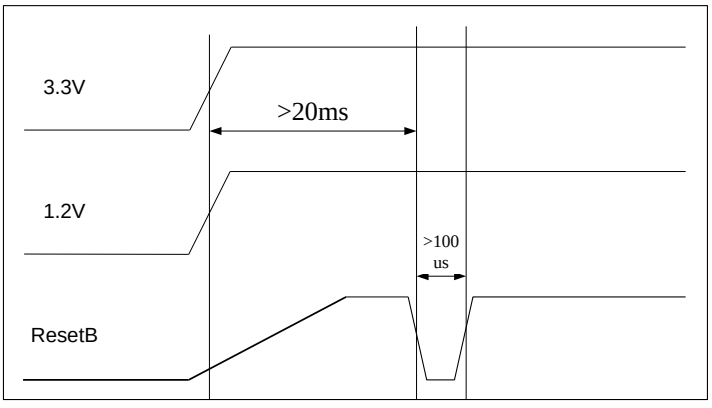

Figure 4: Power-on Reset Function's Sequence external global reset

• XI, XO

27MHz crystal can be connected to these pins of XI, XO as the CH7525 optional reference clock input. In PCB design, 27MHz crystal must be placed as close as possible to the XI and XO pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7525, it is very important that noise should not couple into these input pins.
The crystal load capacitance, CL, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors, **Figure 2** shows a reference design for crystal circuit design.

2.4 Serial Port Control Pins

• SPC and SPD

SPC and SPD function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC pins are pulled up to AVCC (+3.3V) with 6.8kΩ resistors as shown in **Figure 5**. The 22pf capacitor can be used to decrease noise interference. Through these two pins, the firmware can be upgrade into the internal flash memory. If not used in design, they can be either pulled high or pull low with the resistors.

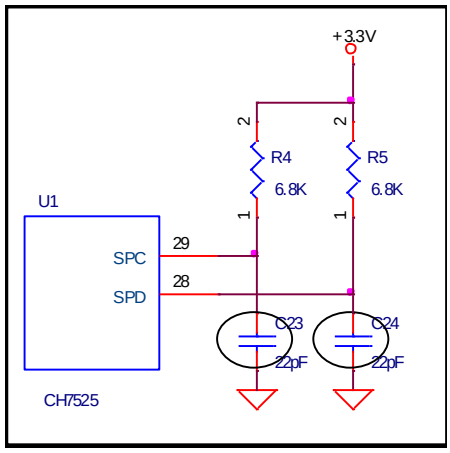

Figure 3: Serial Port Interface

2.5 Display Port Signal Pins

• DP0P/N, DP1P/N, DP2P/N, DP3P/N

These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
Since the digital serial data of the CH7525 may be toggled at speeds up to 2.7 GHz, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7525 should be kept as short as possible and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches. Bend which is smaller than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the source, as shown in **Figure 6**.

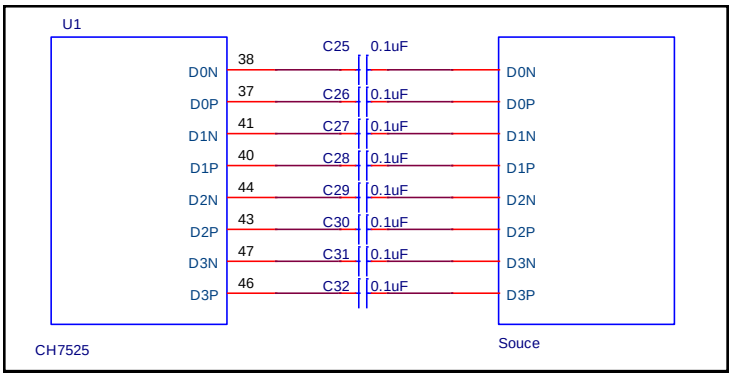

Figure 4: CH7525 DP Main Link Lane Inputs

• AUXP and AUXN

These two pins are DisplayPort AUX channel control that accepts a half-duplex, bi-directional AC-coupled differential signal.
They must have the AC-coupling capacitors, and 100nF capacitors are recommended in this document, as shown in **Figure 7**.

• HPD

This output pin indicates whether this device is active or not. It also generates interrupt pulse as defined by DisplayPort standard. Output voltage is 3.3V. A resistor more than 100K-Ohm should be connected between this pin and GND, as shown in **Figure 7**.

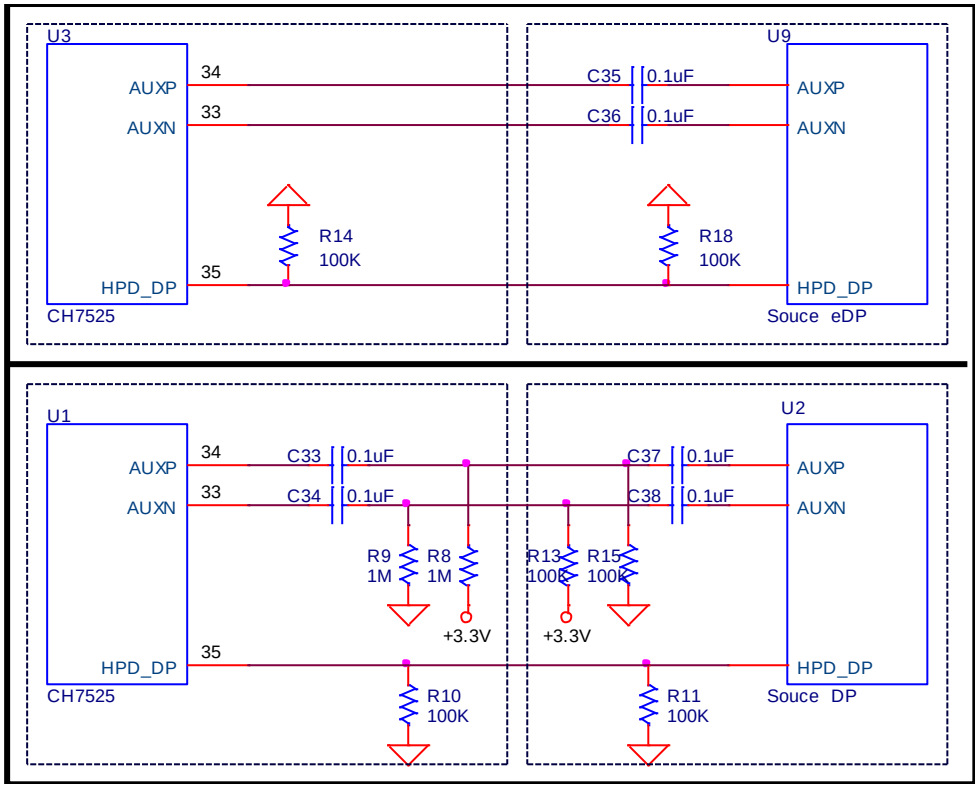

Figure 5: CH7525 AUX channel and HPD

2.6 HDMI Output Pins

• TXC-/TXC+, TX0-/TX0+, TX1-/TX1+, TX2-/TX2+

The TXC-/TXC+, TX0-/TX0+, TX1-/TX1+, TX2-/TX2+ signals are high frequency differential signals that need to be routed with special precautions. Since those signals are differential, they must be routed in pairs.

2.6.1 Differential Pair Impedance

To match the external cable impedance and maintain the maximal energy efficiency it is important to meet the impedance target of 100-Ω ± 10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thickness, board dielectric, etc. The HDMI differential pairs should be routed on the top layer directly to the HDMI connector pads if possible.

2.6.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized; inductive effects may be introduced, causing spikes in the signals. Trace routing lengths from CH7525 to the HDMI connector are limited to a maximum of 2 inches. The CH7525 should be as close to the HDMI connector as possible.

2.6.3 Length Matching for Differential Pairs

The HDMI specifies the intra-pair skew and the inter-pair skew as in **Table 2**. The intra-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between the true and complement signals. The inter-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between any two single-ended data signals that do not constitute a differential pair.

Table 2: Maximum Skews for the HDMI Transmitter

Skew Type	Maximum at Transmitter
Intra-Pair Skew	0.15 T_{bit}
Inter-Pair Skew	0.20 T_{Pixel}

Where T_{bit} is defined as the reciprocal of Data Transfer Rate and T_{Pixel} is defined as the reciprocal of Clock Rate. Therefore, T_{Pixels} is 10 times T_{bit}. In other words, the intra-pair length matching is much more stringent than the inter-pair length matching.

It is recommended that length matching of both signals of a differential pair be within 5 mils. Length matching should occur on a segment-by-segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 100 mils.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

2.6.4 ESD Protection for HDMI Interface

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each HDMI output (data and clock).

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel recommended diode protection circuitry, using BCD AT1140 diode array devices, will protect the CH7525 device from HDMI transmitter discharges of greater than 19kV (contact) and 20kV (air). The

AT1140 have a typical capacitance of only 0.50pF between I/O pins. This low capacitance won't bring too much bad effect on HDMI eye diagram test.

Figure 8 show the connection of HDMI connectors, including the recommended design of AT1140 diode array devices. HDMI connector is used to connect the CH7525 HDMI outputs.

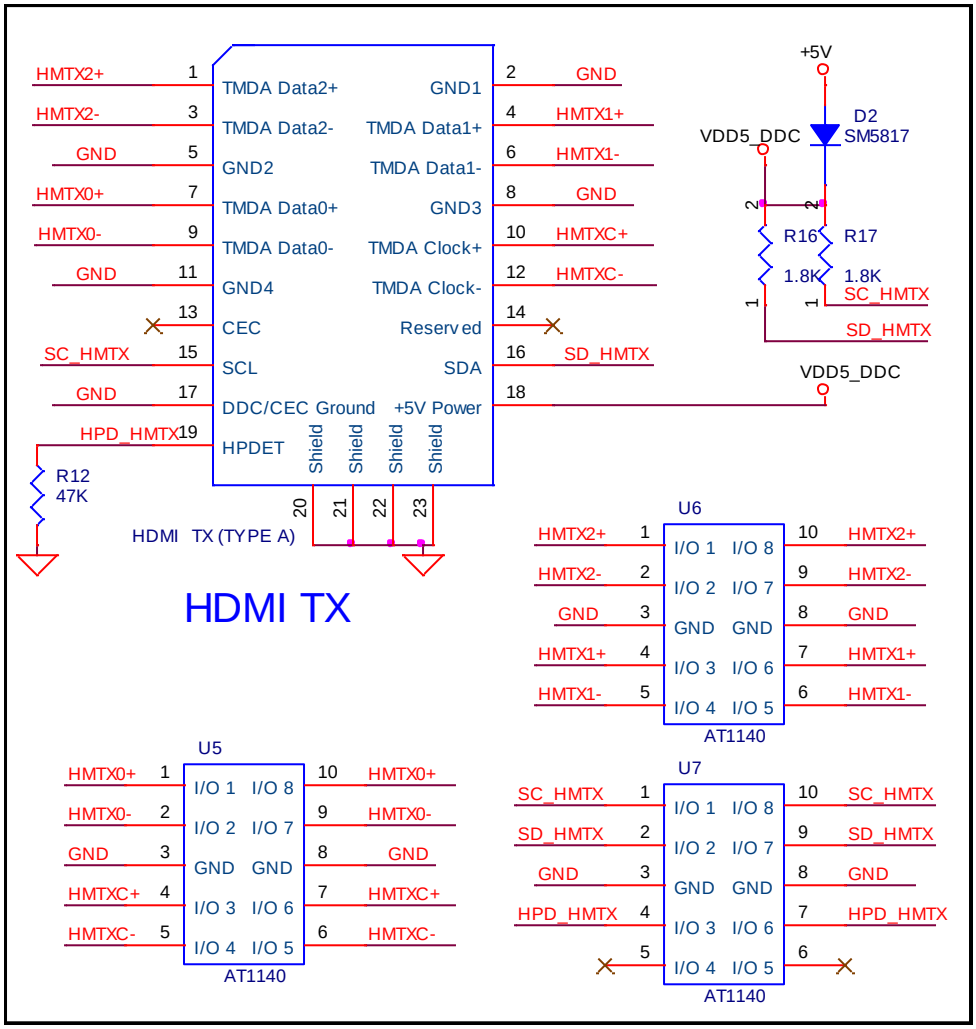

Figure 8: The connection of the HDMI outputs

• HPD_HMTX

This output pin connects to the GND through a 47KΩ resistor. Refer to **Figure 8** for the design example.

2.7 Audio Output

The CH7525 supports up to 8-channel audio input from DP Rx and output from HDMI Tx with sample rate up to 192 KHz. Available audio bandwidth depends on the pixel clock frequency, the video format timing, and whether or not content protection re-synchronization is needed.

2.8 Thermal Exposed Pad Package

The CH7525 is available in 48-pin QFN package with thermal exposed pad package. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7525.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 9.**

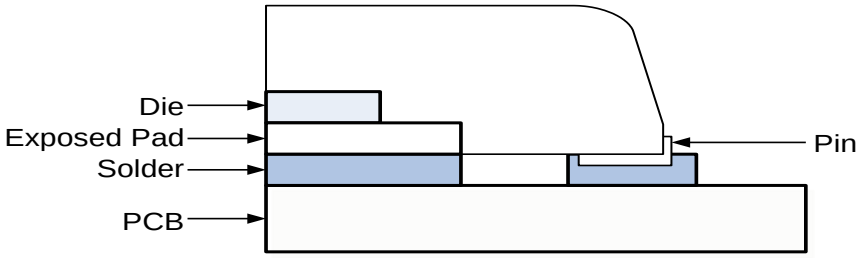

Figure 9: Cross-section of exposed pad package

Thermal pad dimension is from 4.35mm to 4.65mm (min to max), 4.35mm x 4.35mm is the minimum size recommended for the thermal pad, and 4.65mm x 4.65mm is the maximum size. As shown in **Figure 10**, the thermal land pattern should have a 4x4 grid array of 0.9 mm pitch thermal vias connected to the ground layer of the PCB. These vias should be 0.3mm in diameter with 1 oz copper via barrel plating.

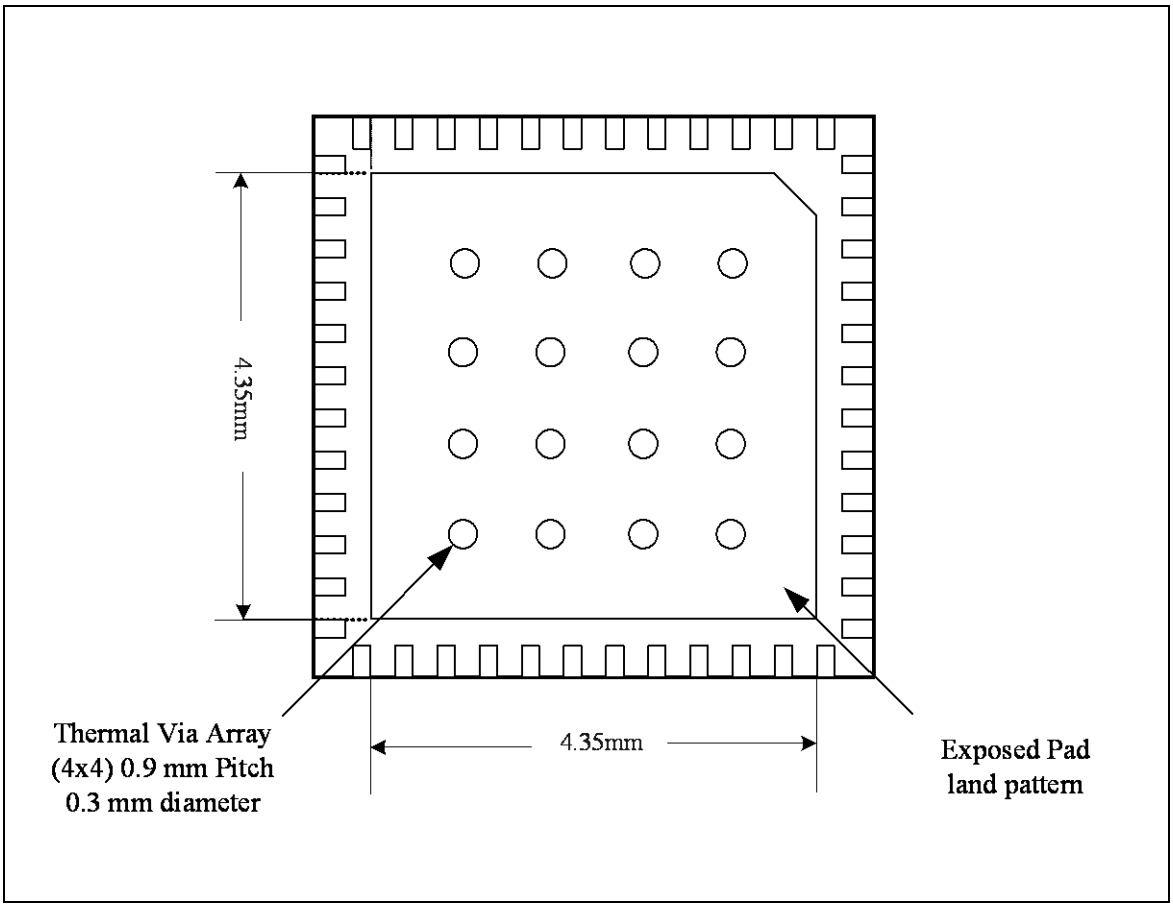

Figure 10: Thermal Land Pattern

3.0 REFERENCE DESIGN EXAMPLE

The following schematics are to be used as a CH7525 PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7525 and would like to have a complete reference design schematic, which should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example

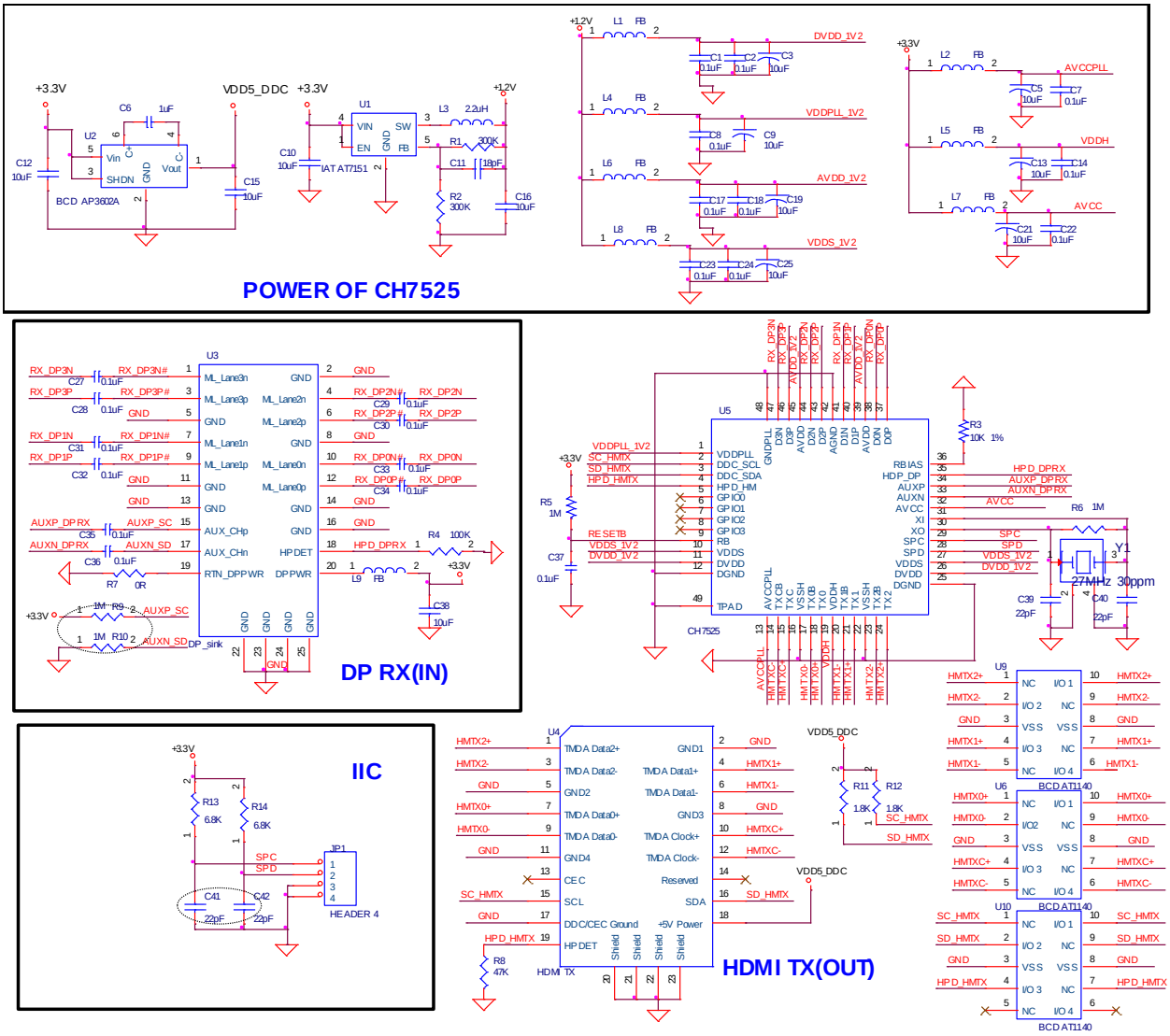

Figure 10: CH7525 Reference schematic

3.2 Reference Board Preliminary BOM

Table 2: CH7517 Reference Design BOM List

Item	Quantity	Reference	Part
1	21	C1, C2, C7, C8, C14, C17, C18,	0.1uF
		C22, C23, C24, C27, C28, C29,	
		C30, C31, C32, C33, C34, C35,	
		C36, C37	
2	12	C3, C5, C9, C10, C12, C13, C15,	10uF
		C16, C19, C21, C25, C38	
3	1	C6	1uF
4	1	C11	18pF
5	4	C39, C40, C41, C42	22pF
6	8	L1, L2, L4, L5, L6, L7, L8, L9	FB
7	1	L3	2.2uH
8	2	R1, R2	300K
9	1	R3	10K 1%
10	1	R4	100K
11	4	R5, R6, R9, R10	1M
12	1	R7	0
13	1	R8	47K
14	2	R11, R12	1.8K
15	2	R13, R14	6.8K
16	1	U1	IAT AT7151
17	1	U2	BCD AP3602A
18	1	U3	DP_sink
19	1	U4	HDMI TX
20	1	U5	CH7525A
21	3	U6, U9, U10	BCD AT1140
22	1	Y1	27MHz

4.0 REVISION HISTORY

Table 3: Revisions

Rev. #	Date	Section	Description	
0.1	2014/05/27	all	Create	
0.2	2014/05/29	2.5 3.0	Modify Aux reference schematic Update reference schematic	
0.3	2014/05/30	2.6 2.8	Modify HDMI reference schematic Add the thermal land pattern	
0.4	2015/04/02	2.5	Modify Figure 7 AUX connection	
0.5	2017/04/27	2.2,2.3	Add power on and off description	
1.0	2020/07/15	2.3	Update the Power-on sequence	

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